Lecture 25: Variable Frequency Oscillator. Gain Limiting

The VFO is one of the main subsystems in a transceiver. It sets the operating frequency for both reception and transmission. In order to "tune" to other frequencies, we actually change the frequency of this *variable* frequency oscillator.

Two general methods for making variable oscillators are:

1. Begin with a crystal oscillator and pass the signal through dividing or multiplication circuits to create sinusoids at other frequencies. This is called a synthesized source (like your Agilent 33120A).
2. Using an LC oscillator with a variable C and/or L.

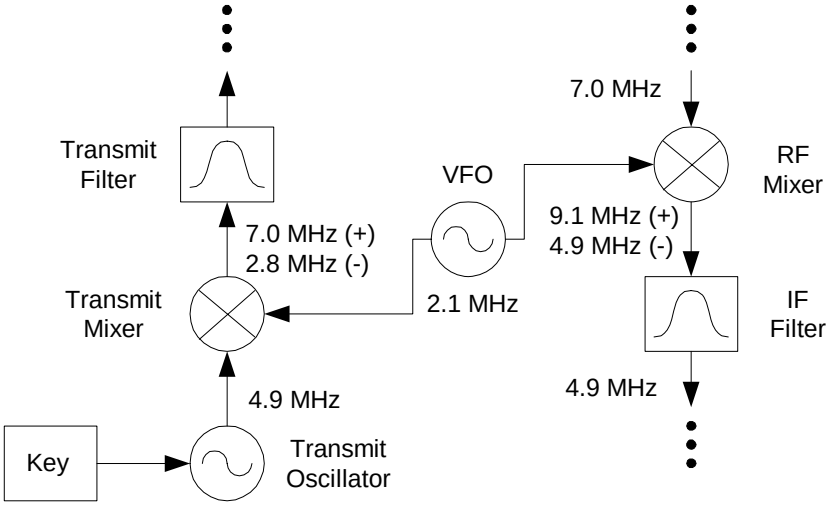
Synthesized sources often are very stable wrt temperature and other climate effects. However, these circuits are generally complex and expensive.

LC oscillators are often cheaper but can be less stable with temperature, humidity and other environmental changes. Our VFO uses a varactor in an LC oscillator to tune frequency.

It is important that once a frequency is set for communication, the transceiver frequency should not vary (at least not too much).

Frequency Drift

In the NorCal 40A, the VFO operates at 2.1 MHz and is used as an input to the Transmit and RF Mixers (see Fig. 1.13):



One reason for choosing a relatively "low" VFO frequency is that frequency drift is proportional to operating frequency. Hence, a lower *f* produces a smaller *f* drift per ºC change.

Also, note that the VFO circuitry in the NorCal 40A is physically as far away as possible from the Power Amplifier. The PA generates most of the heat in the transceiver.

The temperature coefficient α of some quantity x is defined as

$$\alpha = \frac{1}{x}\frac{dx}{dT} \quad [^{o}C]^{-1} \tag{11.26}$$

where T is the temperature (usually ºC).

Your text lists temperature coefficients for many NorCal 40A components in Tables D.1 and D.2 on p. 356. (You can also find these coefficients in component data sheets.)

For example:

- T68-7 core (for L9) has $\alpha = +50$ ppm/ºC,
- Polystyrene capacitors (C51-C53) have $\alpha = -150$ ppm/ºC.

Note that ppm = parts per million = $\frac{\text{Hz}}{\text{MHz}}$ for our purposes.

These four components in the VFO have oppositely signed temperature coefficients! Consequently, these two competing effects help to reduce the frequency drift caused by temperature changes.

Plus, polystyrene capacitors are largely immune to humidity changes.

Apparatus for Problems 27 and 29

In Prob. 27, you will measure the temperature coefficient α for your VFO, and make an estimate of the expected value.

An apparatus has been constructed to enclose your PCB when making these α measurements. Warm your PCB with the heat

gun through the holes on the sides of the container. Be careful not to melt the plastic container. To help with this, hold the heat gun back about 1 foot and wave it back and forth.

Gain Limiting

The VFO in the NorCal 40A is a Clapp oscillator, as shown in Fig. 11.4 and discussed in the last lecture. However, it turns out that the JFET amplifier is **not** overloaded, as sketched in Fig. 11.1(b), in order to obtain the gain condition $|G| = |L|$ for oscillation.

Instead, there is special gain limiting circuitry that has been added to the VFO to keep the JFET from overloading, but still allows the gain to vary with power level.

This gain limiting circuit is formed from the diode, startup resistor and the divider capacitors C_1 and C_2 shown in Fig. 11.6:

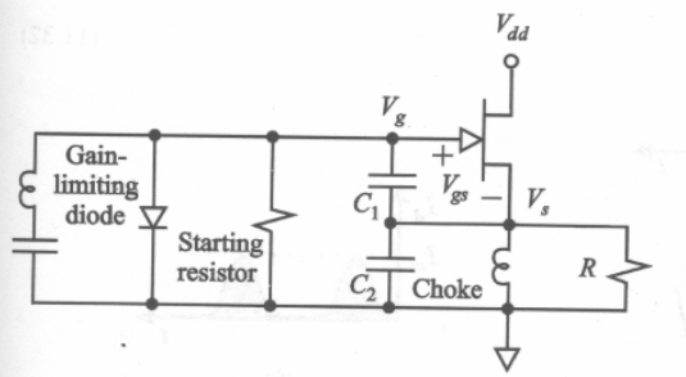
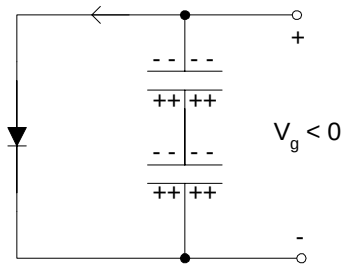


Figure 11.6. The VFO circuit in the NorCal 40A. The choke sets the DC source voltage to zero. The diode limits g_m to give a clean sine wave.

The purpose of the additional components are:

- Startup resistor (R21 = 47 kΩ): When the NorCal 40A is turned on, R21 ensures that the initial gate voltage is zero. This provides a large g_m so that the oscillator starts easily [$g_m > 1/R$ from (11.25)].
- Choke (RFC2 = 1 mH): This forces the DC value of the output voltage V_s equal to zero.
- Gain limiting diode (D9 = 1N4148): This diode only conducts for short periods of time when the sinusoidal gate voltage V_g is near positive peaks.

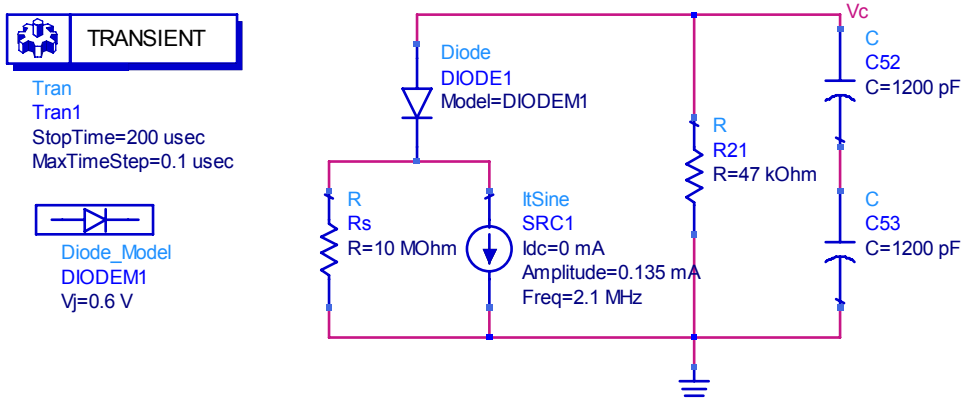
Considering this last component more carefully, when D9 conducts, current flows up through the divider caps C_1 and C_2, and then down through D. Consequently, charge is pulled from the caps leaving them with a net charge per cycle. This provides a negative **dc** voltage on the gate:



The caps will discharge through the startup resistor, but that time constant τ is much greater than T (=1/f = 1/2.1 MHz).

Gain Limiting Circuit Simulation

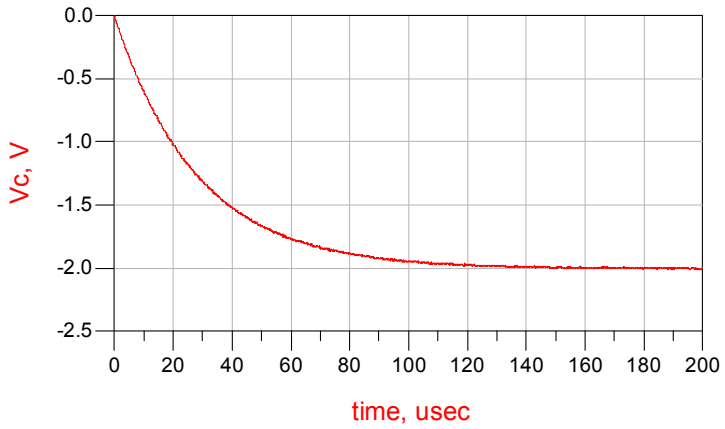
The gain of the JFET amplifier Q8 in the VFO is limited by the circuit shown in Fig. 11.6. In a simulation of the VFO circuit here, we're going to use the ItSine transient current source in ADS, which is zero for $t < 0$ and a sinusoid for $t > 0$. This current source does not appear in the NorCal 40A VFO, and is used here only to illustrate how the capacitors C52 and C53 are charged up for gain limiting purposes.



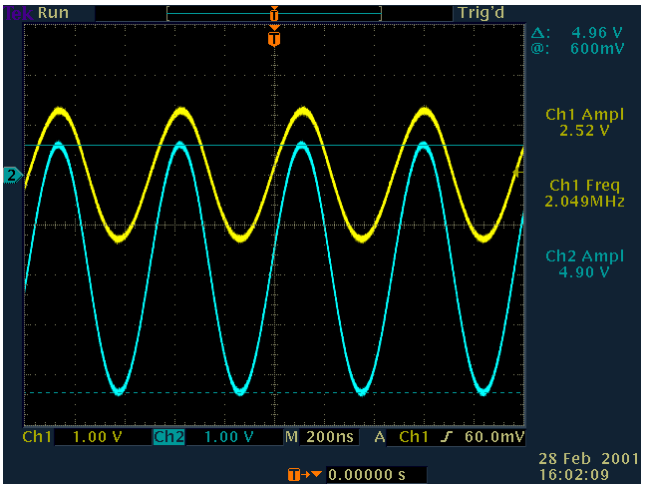
The intended operation of this gain limiting circuit is for the ideal diode DIODE1 to conduct only for positive peaks in I1.

The capacitors slowly charge up and over many periods of the current source reach a steady negative voltage, which is precisely what is needed to limit the gain of Q8.

In the following result, we can see that the voltage across the two capacitors indeed becomes negative and constant with time:



Here are measurements from the actual VFO in the NorCal 40A:



The yellow trace is the source voltage of Q8, while the blue trace is the gate voltage. Note that this latter voltage has a negative average value, as predicted.

Operation of the Gain Limiting VFO Circuit

1. As long as $g_m > 1/R$, the oscillation grows.

2. As the diode conducts current, it pulls charge through C_1 and C_2 thus reducing V_g (< 0) further.

3. As V_{gs} becomes more negative, g_m decreases, as shown in Fig. 11.7(a):

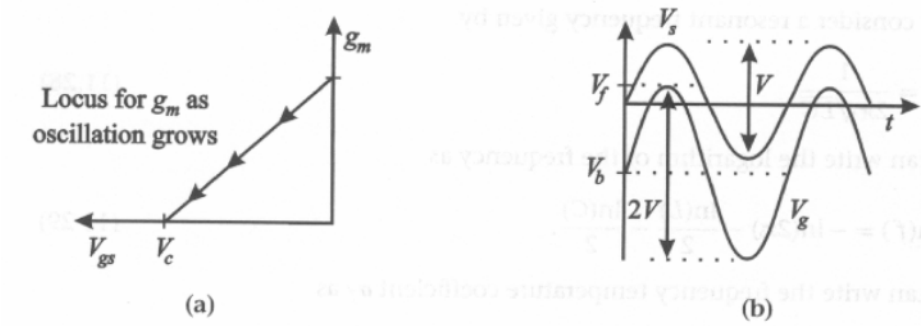


Figure 11.7. Effect of the gain-limiting diode on g_m as the oscillation builds up (a). V_g and V_s waveforms (b).

4. Eventually equilibrium is reached when the oscillation conditions $|G| = |L|$ and $\angle G = \angle L$ are satisfied. In this state, the output voltage oscillates and neither increases in amplitude nor decreases.

VFO Large Signal Analysis

The steady-state JFET source and gate voltages are sketched in Fig. 11.7(b) above. This can be directly compared with the oscilloscope screen shot shown on page 7.

As shown in the text, the large-signal oscillation condition is

$$G_m = \frac{1}{R} \ [\text{S}] \qquad (11.35)$$

where G_m is the large-signal transconductance of the JFET amplifier. It is defined as

$$G_m = \frac{I_{d,\text{pp}}}{V_{\text{gs,pp}}} \qquad (11.34)$$

where $I_{d,\text{pp}}$ and $V_{gs,\text{pp}}$ are peak-to-peak values of the fundamental components (i.e., Fourier terms with frequency = $1 \cdot \omega$) of the drain current and the gate-to-source voltage, respectively.

Our task now is to compute the p-t-p values of these fundamental frequency components so we can determine G_m.

In our VFO, $C_1 = C_2$ so that from (11.23)

$$V_g = 2V_s$$

Because of the choke, V_s has zero dc value, whereas V_g has a dc value of V_b (< 0) due to the gain limiting circuit.

It turns out that V_b is smaller than the pinch off voltage V_c of the JFET, as shown in Fig. 11.8(a):

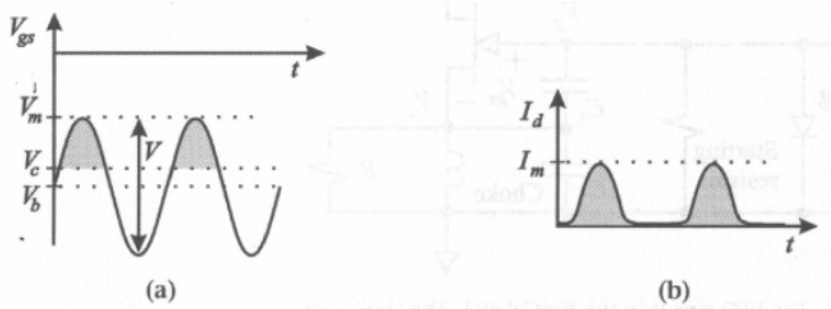


Figure 11.8. VFO gate-source voltage V_{gs} (a), and drain current I_d (b).

Consequently, this amplifier is operated in class C! The transistor is either on or off.

If we approximate V_{gs} as

$$V_{\text{gs}} = \begin{cases} V_m \cos(\omega t) & t_0 \le t \le t_0 + T \\ 0 & \text{otherwise} \end{cases}$$

then during the "on" times of the JFET

$$I_d = I_{\text{dss}}\left(1 - \frac{V_{\text{gs}}}{V_c}\right)^2 \approx \underbrace{I_{\text{dss}}\left(\frac{V_m}{V_c}\right)^2}_{\equiv I_m} \cos^2(\omega t)$$

It is this cosine-squared shape that is sketched above in Fig. 11.8(b).

The dc value of the drain current I_o in the VFO JFET is

$$I_o = \frac{1}{T}\int_{t_0}^{t_0+\frac{T}{2}} I_m \cos^2(\omega t)\, dt$$

or $$I_o = \frac{I_m}{T}\frac{1}{2}\Big|_{t_0}^{t_0+\frac{T}{2}} = \frac{I_m}{4} \qquad (11.37)$$

As shown in Section B.4 from a Fourier series expansion of a cosine square function, the p-t-p amplitude of the fundamental component is four times the dc value:

$$I_{d,\text{pp}} = 4 \cdot I_o \underset{(11.37)}{\approx} I_m \qquad (11.38)$$

In words, (11.38) means that the p-t-p fundamental current component (i.e., a 2.1-MHz sinusoidal current) of the VFO JFET drain current, $I_{d,\text{pp}}$, is simply equal to I_m.

Now, we divide (11.38) by $V_{s,\text{pp}}$, which is the p-t-p output (i.e., JFET source) voltage and find

$$\boxed{G_m = \frac{I_{d,\text{pp}}}{V_{s,\text{pp}}} = \frac{I_m}{V_{s,\text{pp}}}} \qquad (11.39)$$

Fig. 11.9 contains a plot of (11.39) using (11.33), and (apparently) I_{dss} and V_c for some particular JFET:

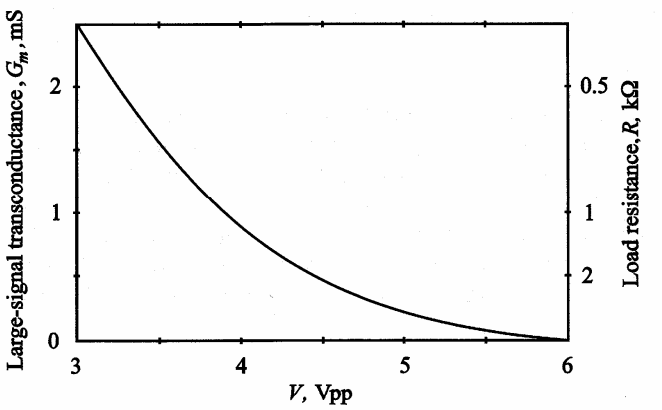


Figure 11.9. Large-signal transconductance G_m of the J309 JFET in a Clapp oscillator with $C_1 = C_2$. V is the peak-to-peak value of both the gate-source voltage and the output voltage. The right axis gives the load resistance R on an inverted scale to allow prediction of the output voltage.

In Prob. 27.B you will use Fig. 11.9 to predict $V_{s,\text{pp}}$ for a particular load resistance (since $G_m = 1/R$). (I didn't obtain very good results for this part.)