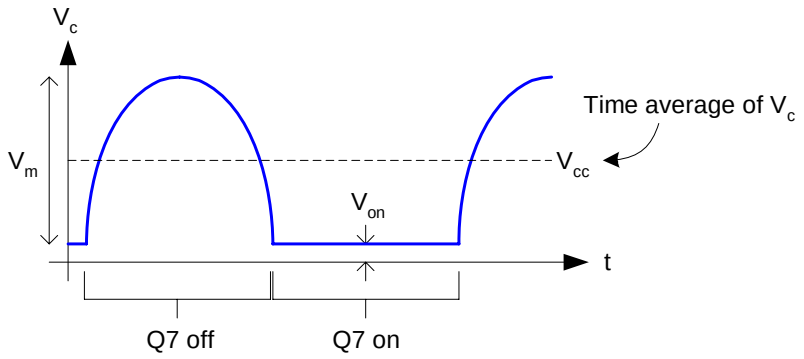
Lecture 23: NorCal 40A Power Amplifier. Thermal Modeling.

Recall from the last lecture that the NorCal 40A uses a Class C power amplifier. From Fig. 10.3(b) the collector voltage was modeled as



The transistor Q7 in the amplifier is either "off" (cutoff) or "on" (saturated). In-between these times, the transistor is active for a short time. (We'll consider the active regions shortly.)

Also, we computed the maximum collector voltage to be

$$V_m = \pi\left(V_{cc} - V_{on}\right) \tag{10.3}$$

and the maximum efficiency of the power amplifier to be

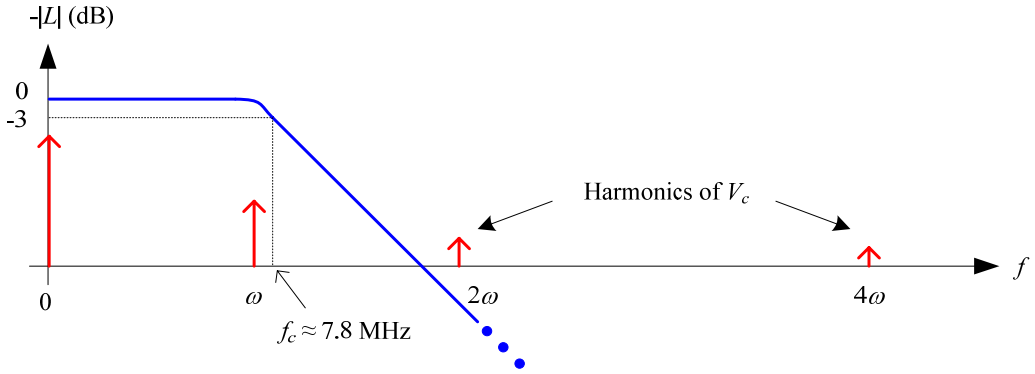
$$\eta_{max} = 1 - \frac{V_{on}}{V_{cc}} \tag{10.7}$$

The last Class C power amplifier characteristic we need to compute is the ac output power P delivered to the load. The load in this case is the antenna, which is connected at the output of the Harmonic Filter.

From (10.6), $P=\left(V_{cc}-V_{on}\right)I_o$. But I_o is unknown. On the other hand, V_c **is** known. So, let's compute the Fourier series expansion of V_c shown in Fig. 10.3(b). Using the analysis given in Appendix B, Section 3:

$$V_c(t)=\underbrace{V_{cc}}_{\text{DC}}+\underbrace{\frac{V_m}{2}\cos(\omega t)}_{\text{fundamental}}+\underbrace{\frac{2V_m}{\pi}\left[\frac{\cos(2\omega t)}{3}-\frac{\cos(4\omega t)}{15}+\frac{\cos(6\omega t)}{35}-\cdots\right]}_{\text{higher-order harmonics}} \tag{10.8}$$

Recall that in Prob. 15 you designed the Harmonic Filter to be a fifth-order, low-pass ladder filter:



When the NorCal 40A is transmitting, the Harmonic Filter reduces the "higher-order harmonic" content in V_c (10.8) by significantly attenuating these frequency components.

We'll assume that these higher-order harmonics (2ω, 4ω, 6ω…) are completely attenuated by the Harmonic Filter and do not

appear at the antenna. This is a good assumption if you observe the oscilloscope screenshot shown in the previous lecture.

With this background information, we are now able to calculate the output signal (ac) power P. Assuming a lossless Harmonic Filter at f_{rf}, then in terms of the phasor antenna voltage, V:

$$P = \frac{1}{2}\frac{V^2}{R}$$

where R is the antenna input resistance (ohmic plus "radiation").

From the second term in (10.8), the amplitude of the fundamental harmonic in the output voltage is $V_m/2$ so that

$$P = \frac{1}{2}\frac{\left(V_m/2\right)^2}{R} \underset{(10.3)}{=} \frac{\pi^2\left(V_{\text{cc}} - V_{\text{on}}\right)^2}{8R} \quad [\text{W}] \qquad (10.9)$$

We can use this equation to compute the signal power delivered to the antenna (with an input resistance of R) when driven by the Class C power amplifier in the NorCal 40A. Nice!

So how can we increase the ac output power P? (This is important, after all, since this will be the power delivered to our propagating electromagnetic wave launched by the antenna.)

1. Increase the dc supply voltage V_{cc}. We can't exceed the specs of the transistor, though, or will cause a failure.
2. Decrease R of the antenna. This has a limited effect, though, since as $R\downarrow$, $I_o\uparrow$ which implies that $V_{\text{on}}\uparrow$ (the saturation voltage of Q7).

Class C Amplifier Transistor Losses

It is interesting to examine the losses in the transistor. From measurements on a NorCal 40A recorded in the text on p. 185, P = 2.5 W and η = 78 %. Therefore,

$$P_o = \frac{P}{\eta} = \frac{2.5}{0.78} = 3.2 \text{ W}$$

Consequently, the difference

$$P_d = P_o - P = 3.2 - 2.5 = 0.7 \text{ W} \qquad (10.10)$$

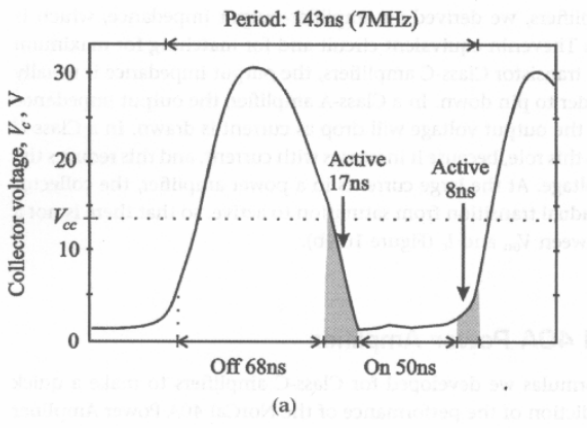
must be the power dissipated in the transistor, P_d.

This P_d has two sources:

1. The brief time when the transistor is in the active mode while the transistor is passing from the off to on states (and to a much lesser degree when passing from on to off), and
2. The "on" period when the transistor is saturated.

We'll carefully examine each of these sources separately.

1. Active-Period Losses. From Fig. 10.5:



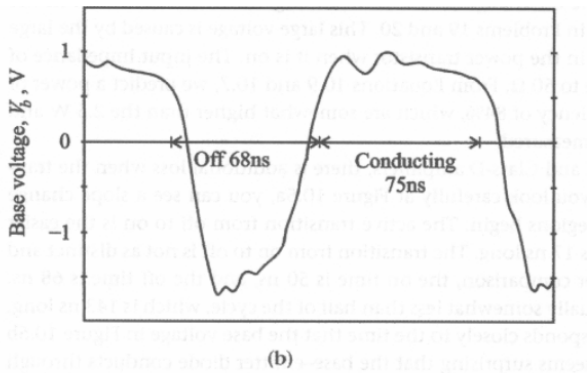
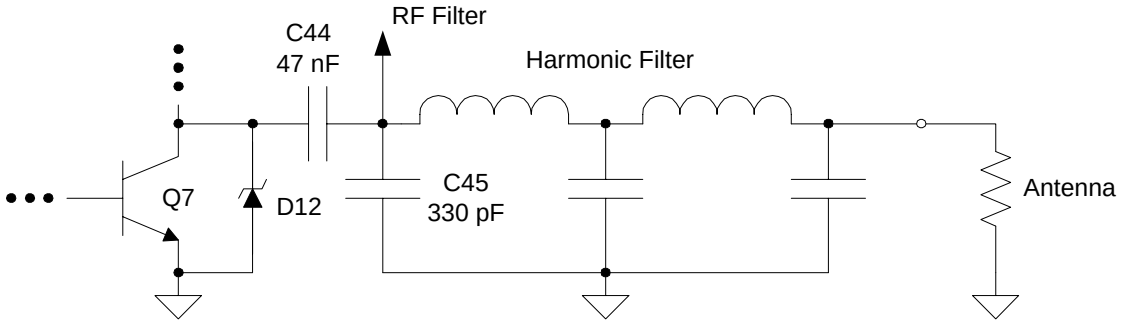


Figure 10.5. Voltages for the NorCal 40A Power Amplifier at 7 MHz. The output power is 2.5 W, with a supply voltage of 12.8 V and a supply current of 250 mA. The efficiency is 78%. Collector voltage (a), and base voltage (b).

Note that the time-varying collector voltage during the off-to-on transition is much larger than during the on-to-off transition. Also observe that this transition time is much longer. Because of these two characteristics, we'll expect the energy losses associated with the off-to-on transition to dominate.

To begin, the active mode loss in Q7 occurs because of so-called "capacitive discharge" through Q7.



This capacitive discharge is due to energy stored in C45 dissipating through Q7. (Note that C44 is a dc blocking capacitor; hence, the voltage drop across C44 is very small, which implies the stored energy is also small.)

Additional capacitive discharge will come from Q7 itself, D12 and the RF Filter. However, all these turn out to be small wrt C45.

From Fig. 10.5(a) we see that V_c (= V_{C45}) $\approx$15 V at the beginning of the off-to-on transition. The stored energy is then

$$E_1 = \frac{1}{2} C_{45} V_c^2 = 37.1 \text{ nJ} \qquad (10.11)$$

At the end of the transition, $V_c \approx 2$ V so that

$$E_2 = \frac{1}{2} C_{45} V_c^2 = 0.66 \text{ nJ}$$

Therefore, during this off-to-on transition, the change in the stored energy in C45 is

$$\Delta E_{C45} = E_1 - E_2 = 37.1 - 0.7 = 36.4 \text{ nJ}$$

The time **average** power dissipation P_a' associated with capacitive discharge from C45 during the off-to-on transition is

$$P_a' = \frac{\Delta E_{C45}}{T} = (36.4 \text{ nJ}) \cdot f = 255 \text{ mW} \qquad (10.12)$$

for a waveform of frequency f (= 7 MHz) and period T.

Similarly, for the on-to-off transition

$$P_a'' = \frac{1}{2T} 330 \times 10^{-12} \left[6^2 - 3^2 \right] = 31 \text{ mW}$$

The total active-mode loss (time average power) in the power amplifier transistor Q7 is then the sum of these two:

$$P_a \approx P_a' + P_a'' = 286 \text{ mW} \qquad (10.12)$$

2. On-Period Losses. During the "on" period, transistor Q7 is saturated with a collector-to-emitter voltage V_{on}. The average power dissipated during this period P_{on} is

$$P_{on} = V_{on} I_{on} \qquad (10.16)$$

From Fig. 10.5(a) we see that $V_{on} \approx 2$ V. (This is a large saturation voltage compared with the 0.2 V we're accustomed to. Why is V_{on} so large here?)

To calculate I_{on}, use KCL:

$$I_{on} = I_o - I_c \qquad (10.15)$$

where I_o is the average (dc) current from the power supply (measured to be 250 mA) and I_c is the average capacitive discharge current through Q7.

For the off-to-on transition, a stored charge Q is "released." With $Q = CV$, then $\Delta Q = C\Delta V$ so that

$$\Delta Q' = C45 \cdot \Delta V = 330 \times 10^{-12} (15 - 2) = 4.3 \text{ nC}$$

Similarly, for the on-to-off transition,

$$\Delta Q'' = C45 \cdot \Delta V = 330 \times 10^{-12} (6 - 3) = 1.0 \text{ nC}$$

Therefore, $$\Delta Q = \Delta Q' + \Delta Q'' = 5.3 \text{ nC} \qquad (10.13)$$

This discharge of stored charge in Q7 produces the time dependent collector current

$$i_c(t) = \frac{dQ}{dt} \approx \frac{\Delta Q}{\Delta t} \qquad (1)$$

For our dissipated power calculation, we're only interested in the average current associated with this discharge. Using (1), we can approximate this average current as

$$I_c = \langle i_c(t) \rangle \approx \frac{\Delta Q}{T} = \Delta Q \cdot f$$

so that $$I_c = 5.3 \times 10^{-9} \cdot 7 \times 10^{6} = 37 \text{ mA}. \qquad (10.14)$$

Then, from (10.15) $$I_{\text{on}} = 250 - 37 = 213 \text{ mA}$$

Therefore, the total power dissipated in Q7 during the "on" periods is

$$\boxed{P_{\text{on}} = V_{\text{on}} I_{\text{on}} \approx 2 \cdot 213 \times 10^{-3} = 426 \text{ mW}} \qquad (10.16)$$

The total power dissipated by the transistor Q7 is the sum of these two powers (note that no power is dissipated when Q7 is cutoff):

$$\boxed{P_d = P_a + P_{\text{on}} = 286 + 430 = 712 \text{ mW}} \qquad (10.17)$$

Observe that this calculated power dissipation in Q7 is quite close to the measured value of 700 mW calculated in (10.10) at the beginning of this discussion.

Fig. 10.6 contains a diagram of the power flow in the NorCal 40A Power Amplifier.

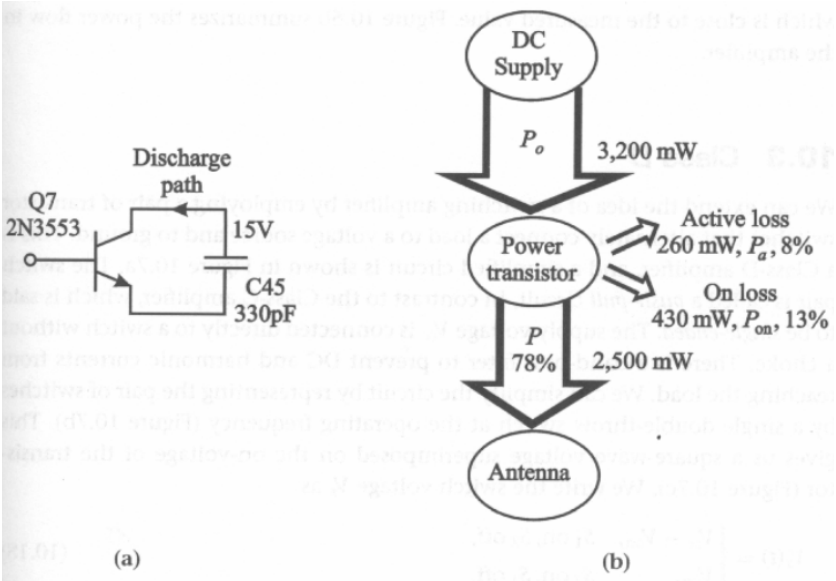


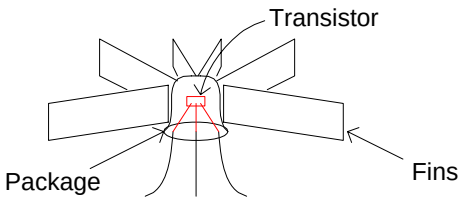
Figure 10.6. (a) Capacitive discharge through the collector of the power transistor. The DC block (C44) is not shown. C45 is charged to 15 V when the active transition begins. (b) The power flow in the NorCal 40A Power Amplifier when the output is 2.5 W.

Thermal Modeling

Power amplifiers often heat up due to the relatively high voltages and currents at which they operate. While this is wasted energy, it is something that often cannot be avoided.

At high temperatures T, solid-state transistors are more likely to fail. It is important to design a heat transfer system (fins, fans, etc.) so that T remains below the maximum rating specified by the transistor manufacturer.

Here we will develop a simple heat transfer model for the transistor, the package and the fins in order to model the transient heat transfer from the transistor to surrounding air.



There are two important properties of materials that are necessary to describe this heat transfer:

1. Thermal resistance, R_t: This material property is defined as

$$R_t = \frac{\Delta T}{P_d} \quad [^\circ\text{C/W}] \tag{10.41}$$

From this expression, we deduce that the dissipated power P_d

$$P_d = \frac{T - T_o}{R_t}$$

is the rate at which heat (energy) is transferred from a body at temperature T to the ambient air at temperature T_o.

Note that for a fixed ΔT, as $R_t \uparrow$, $P_d \downarrow$, and *vice versa*.

2. Thermal capacitance, C_t: This material property is defined as

$$C_t = \frac{Q}{\Delta T} = \frac{\text{heat energy}}{\Delta \text{ temperature}} \quad [\text{J}/^\circ\text{C}] \tag{2}$$

Thermal capacitance is the ratio of the heat Q supplied to a body in any process that creates a temperature change ΔT.

From (2) and dividing by Δt

$$C_t \frac{\Delta T}{\Delta t} = \frac{Q}{\Delta t}$$

Taking the limit of this equation as Δt vanishes

$$\lim_{\Delta t \to 0} \left\{ C_t \frac{\Delta T}{\Delta t} = \frac{Q}{\Delta t} \right\}$$

we obtain

$$\boxed{C_t \frac{dT}{dt} = P_d} \qquad (10.42)$$

Equations (10.41) and (10.42) are the fundamental governing equations for our simplified transistor heating problem.

To help solve such heat transfer problems, it's sometimes useful to apply an electrical circuit analogy. In this analogy, electrical circuit and heat transfer quantities are interchanged as:

$$V \Leftrightarrow \Delta T$$
$$I \Leftrightarrow P_d$$
$$R \Leftrightarrow R_t$$
$$C \Leftrightarrow C_t$$

Applying this analogy, then (10.41) becomes

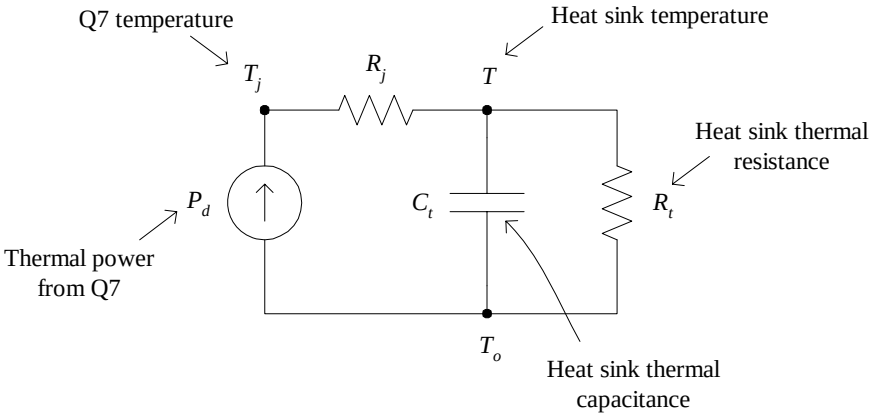
$$R = \frac{V}{I}$$

and (10.42) becomes

$$C \frac{dV}{dt} = I$$

Both of these electrical circuit equations are very familiar to you.

Based on this analogy, we can quickly construct an equivalent **thermal** circuit model for the transistor, package and fin as shown in Fig. 10.15(a):



R_j is the thermal resistance of the transistor-to-package interface. You often find this quantity specified by the manufacturer in the transistor datasheet.

Our goal here is to find equations for the heat sink temperature $T(t)$ and the transistor temperature $T_j(t)$ as functions of time t.

From "KCL" at node T in the thermal circuit above:

$$P_d = \frac{T(t)-T_o}{R_t} + C_t \frac{d\left[T(t)-T_o\right]}{dt} = \frac{T(t)-T_o}{R_t} + C_t \frac{dT(t)}{dt} \qquad (10.53)$$

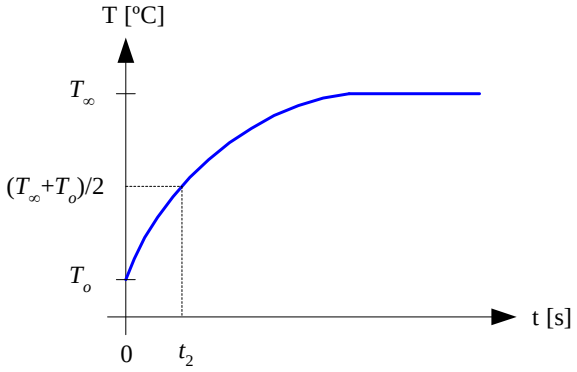
Rearranging this equation we find

$$R_t C_t \frac{dT(t)}{dt} + T(t) = R_t P_d + T_o \qquad (10.54)$$

This is a simple 1-D ordinary differential equation. The solution is

$$T(t) = T_\infty - P_d R_t e^{-t/\tau} \qquad (10.58)$$

where $T_\infty = P_d R_t + T_o$ and $\tau = R_t C_t$ (10.57),(10.56)



The behavior of this thermal circuit (and, consequently, the physical heat transfer phenomenon) is just like a single time constant electrical circuit. Very "cool"!

It turns out that such analogies between electrical and mechanical systems are not uncommon.

In Prob. 25, you will model and measure the thermal characteristics of the power amplifier with its attached heat sink.