Lecture 22: Class C Power Amplifiers

We discovered in Lecture 18 (Section 9.2) that the maximum efficiency of Class A amplifiers is 25% with a resistive load and 50% with a transformer-coupled resistive load.

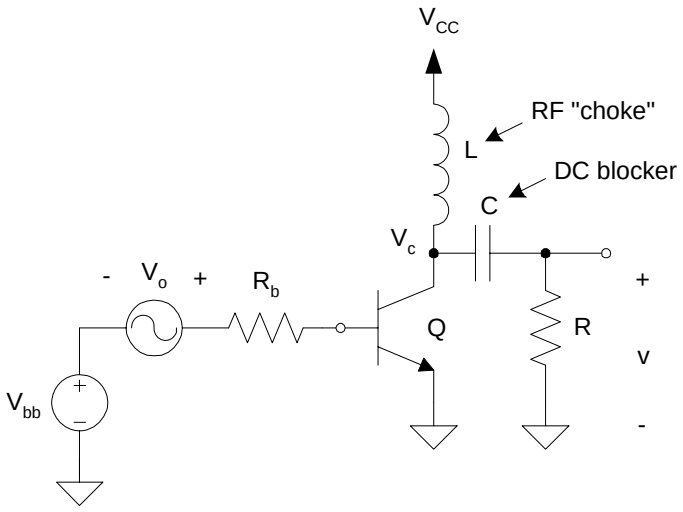
Also, Class A amplifiers dissipate energy (in the transistor) even when there is no RF output signal! (Why?)

So, while the Class A amplifier can do an excellent job of producing linear amplification, it is very inefficient. In this lecture, we will discuss amplifiers with improved efficiency.

RF Chokes

To better understand at least some of these improvements, it will be useful to first examine the effects of an inductor in the collector circuit of a common emitter amplifier with a capacitively-coupled load *R*, as shown in the following figure.

Supposing Class A operation, we can break up the analysis of this circuit into dc and ac parts, as we've done in the past with other linear amplifiers.



I. DC analysis – Referring to the circuit above, note that:

- ✓ We assume V_{bb} was properly adjusted to place Q in the active mode.
- ✓ C is a dc blocking capacitor. This keeps the dc current that is biasing Q from being redirected through R.
- ✓ L has zero (or, at least, a very small) resistance.

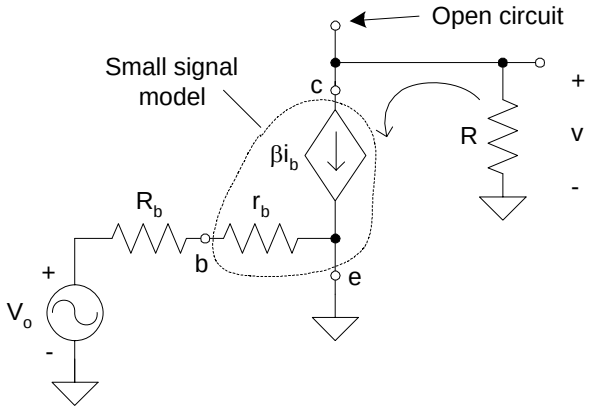
Because L is connected from V_{cc} to the collector, V_c has a time-average value equal to V_{cc}. (This is the same situation we saw with a transformer-coupled load in Class A amplifiers.)

II. AC analysis

In the amplifier above, the inductance is chosen so that L presents a "large" impedance at the frequency of operation. Hence, this inductor is called an RF choke.

Conversely, the impedance of the dc blocking capacitor *C* is very small at RF frequencies.

Consequently, the ac small signal model for this amplifier is:



From this small signal model, we see that the phasor collector voltage is just

$$v = -\beta i_b R$$

The total collector voltage V_c is the sum of these dc and ac components (since this is a linear circuit):

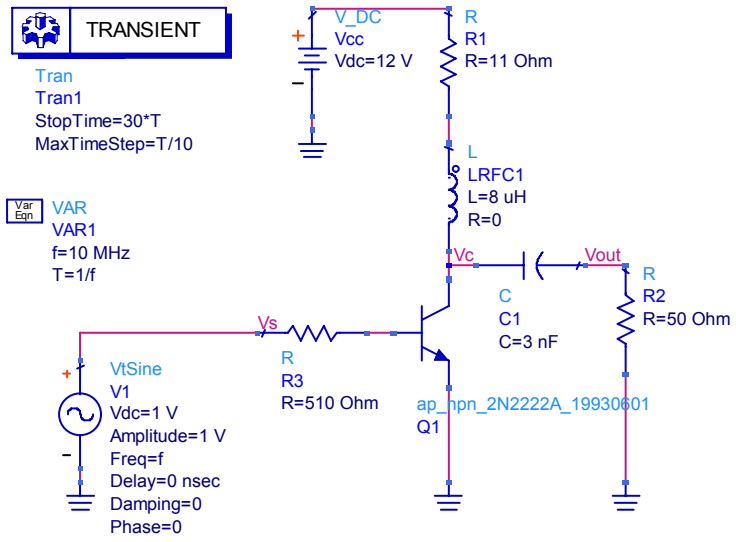
$$V_c(t) = V_{\text{dc}} + V_{\text{ac}} = V_{\text{cc}} - \beta i_b R \cos\left(\omega t + \phi\right) \text{ [V]}$$

Shown next are two ADS simulations of this circuit.

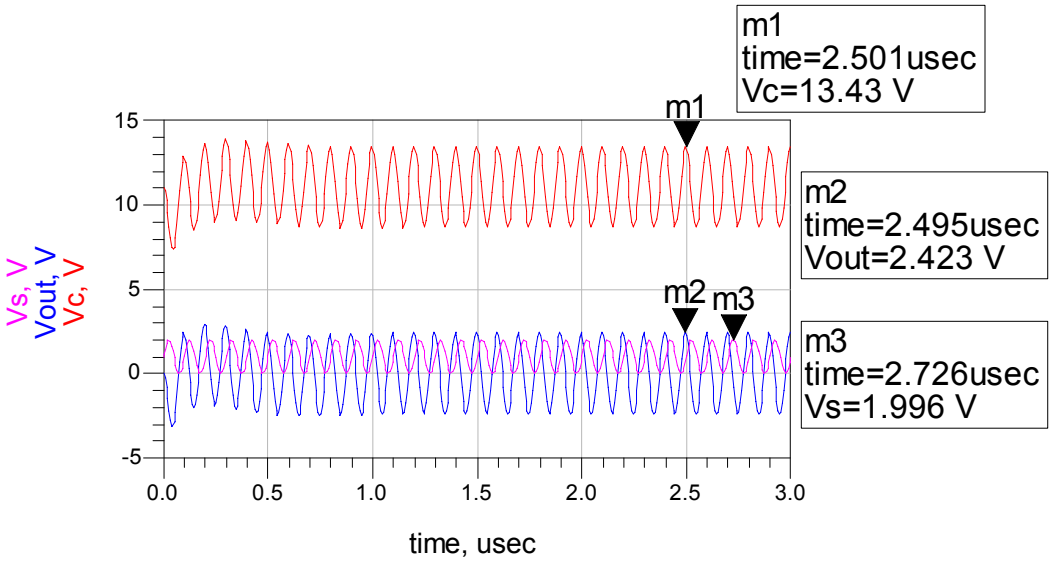
Class A Power Amplifier Simulations

Here we are following Example 12-1.1 from Krauss, Bostian and Raab, *Solid State Radio Engineering* (p. 355). Q1 is biased

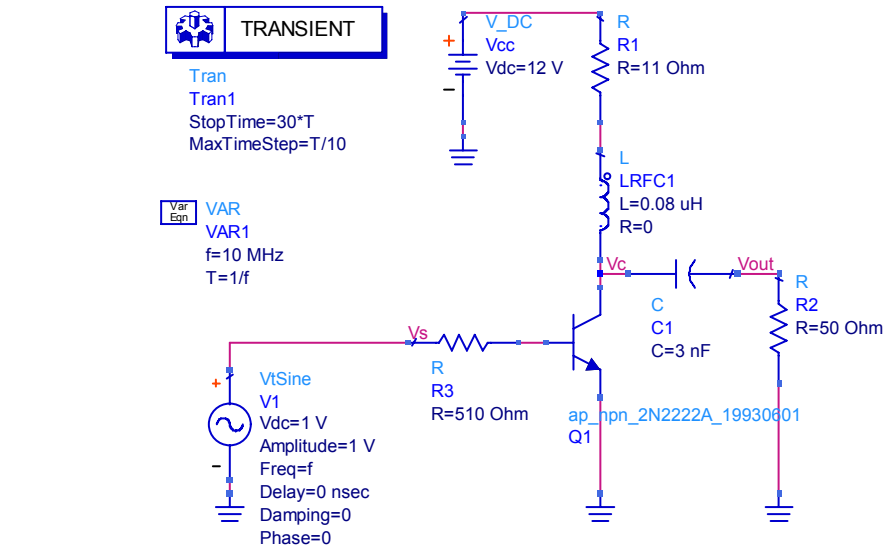
in the active region by V1 and R3. (A parallel LC tank at the output isn't needed to suppress harmonics.) Note that with $f = 10$ MHz, $X_{\text{LRFC1}} = 502.7\ \Omega$, which is greater than $10 \cdot \text{R2}$.

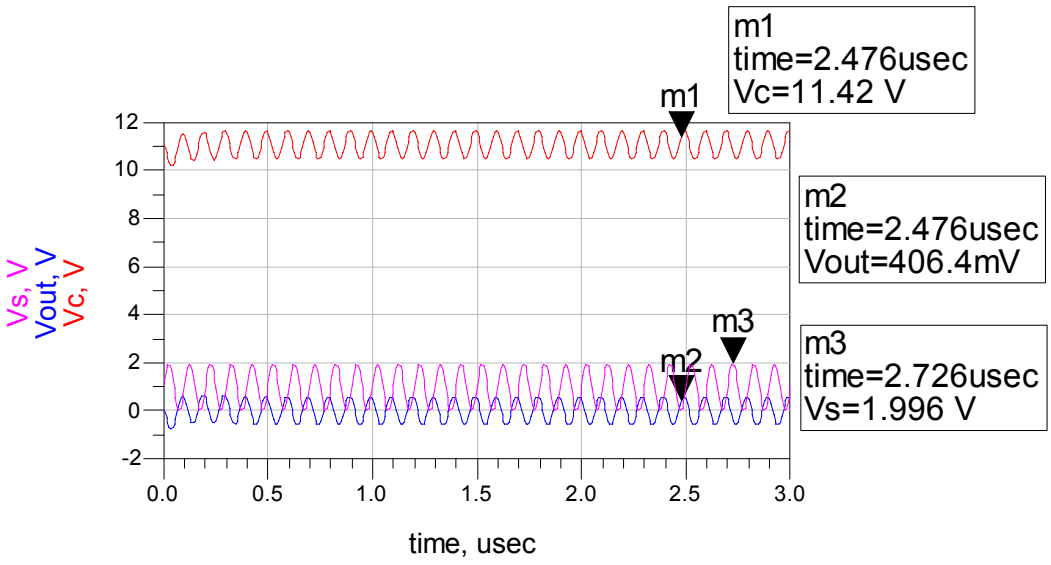


The large impedance of LRFC1 at RF frequencies dictates that the average value of the collector voltage equals Vcc minus the dc voltage drop across R1. This is a new effect, different than what we've seen with other small-signal Class A amplifiers.

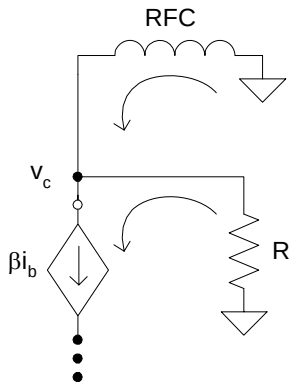


Next, we decrease LRFC1 by 100 times to 0.08 μH. From the simulation results, we see that the average collector voltage is no longer equal to Vcc. In fact, the maximum collector voltage no longer even *exceeds* Vcc (primarily because of the 11-Ω resistor R1).





We see in this second example that if the choke impedance is **not** large, $V_c(t)$ has contributions from both R and L:



Class C Amplifier

The Class A amplifier with a choke, as we just considered, is no more than 25% efficient, which is typical of all Class A amplifiers with directly-coupled resistive loads.

To greatly reduce the power dissipated in the transistor, we will try operating *Q* outside of the active region!

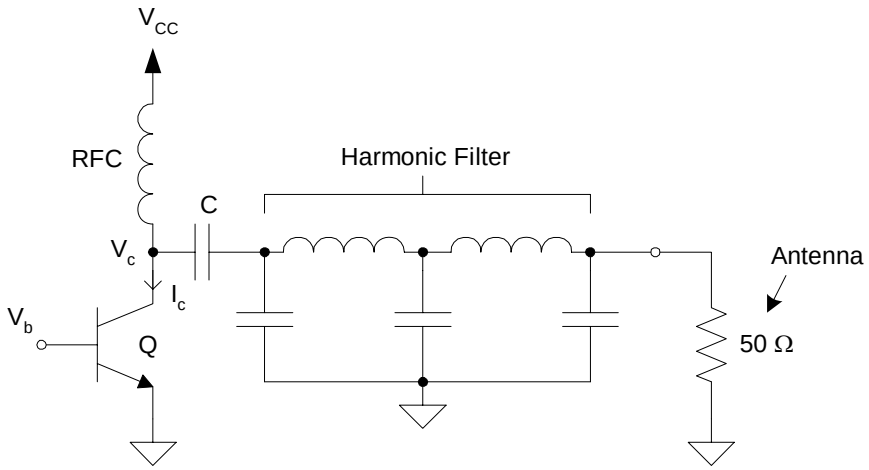
We could greatly increase the efficiency of such an amplifier if we incorporated the following characteristics:

1. To eliminate power dissipation when there is no input signal, we will leave *Q* unbiased.
2. When "on" we will drive *Q* all the way into saturation. This helps reduce the power consumed in *Q* since $V_{CE,sat}$ is low ($\approx 0.1 - 0.2$ V).

This is a cool idea, but unfortunately, it is very nonlinear.

In the NorCal 40A, however, we don't actually need a linear amplifier. A **filtered output** will work just as well. Recall that a CW signal is simply a tone (of a specified frequency) when transmitting, and no signal when not transmitting.

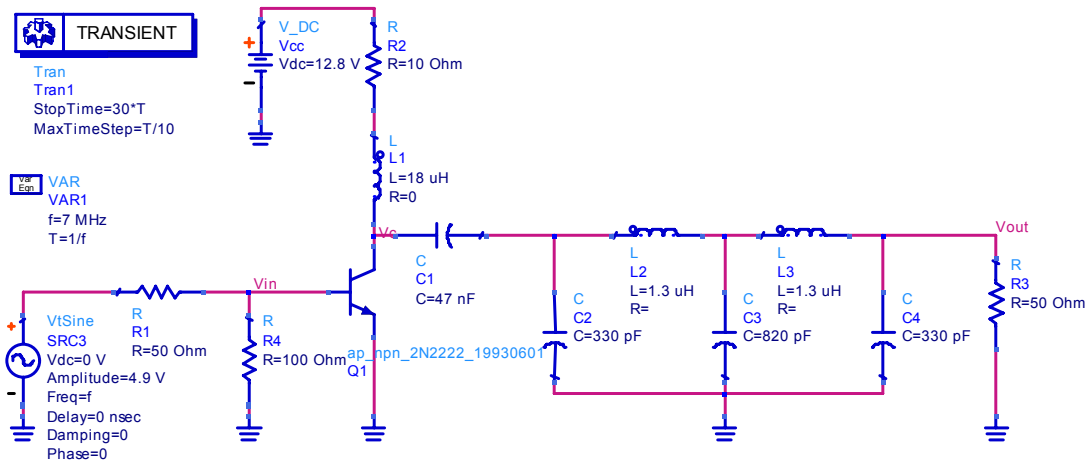
One example of an amplifier with a choke in the collector lead is the Class C amplifier, as shown in Fig. 10.2:



The example below contains a simulation of this amplifier as well as actual measurements from Prob. 24.

Class C Power Amplifier Simulations

Shown here is a simulation of the Class C power amplifier in the NorCal 40A. At this point, stop and ask yourself, "What do I expect the collector voltage to look like?" It turns out that this is difficult to answer since Class C is a highly nonlinear amplifier.



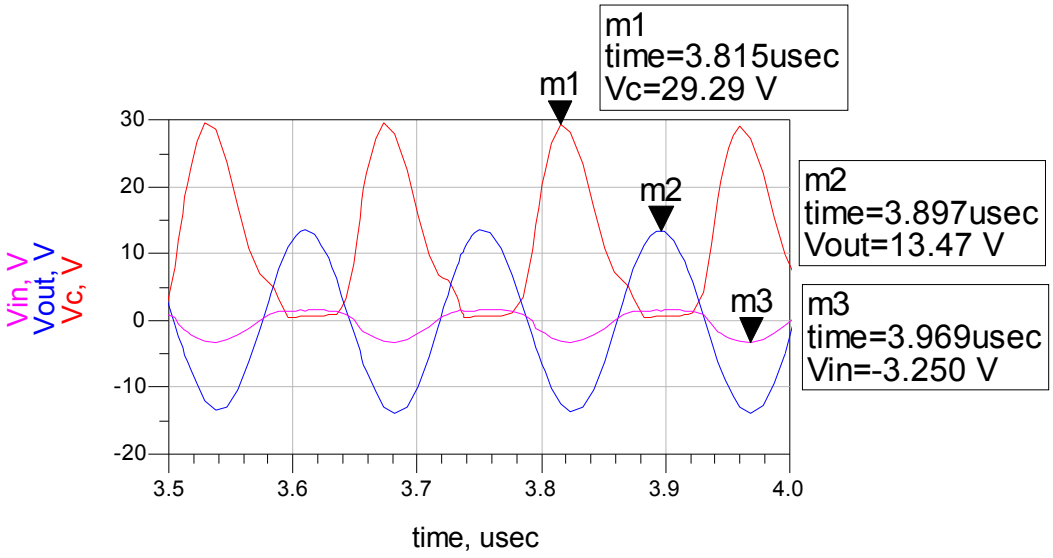
Because this is a highly nonlinear problem:

- We can't use superposition of dc and ac solutions, and
- We can't use a small signal model of the transistor.

So, simulation is probably our best approach to solving this problem. (Note that a 2N2222 transistor is used in this simulation rather than a 2SC799 or 2N3553. The later doesn't work correctly in ADS for some unknown reason. You can't always believe the results from simulation packages!)

Nevertheless, we can use fundamental knowledge about key sections of this amplifier to understand how it should behave, and to develop approximate analytical formulas for its design. We'll take a closer look at this shortly.

In Fig. 10.3(b), the text models the collector voltage as roughly a half-sinusoid. (It's not clear why, though, at that point in the text.) Here are the results from ADS simulation:



It is apparent that the collector voltage Vc is a much more complicated waveform than in a Class A amplifier, when both are excited by a sinusoid.

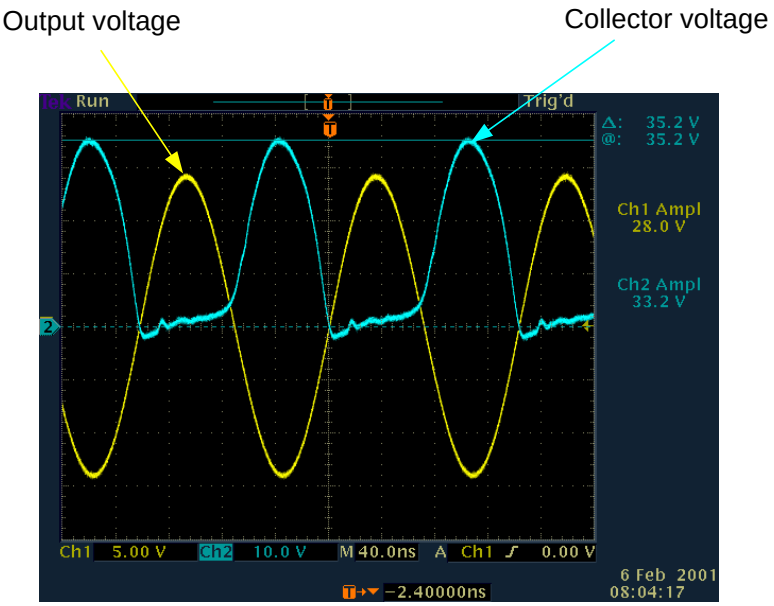
We see in these results that:

(1.) Vc is approximately a half sinusoid when *Q* is "off" (cutoff),

(2.) Vc is approximately zero when *Q* is "on" (saturated), and

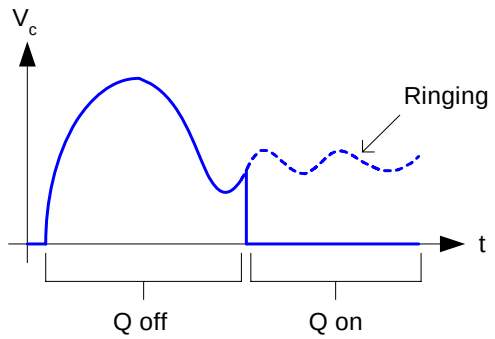
(3.) The base voltage Vin mirrors the input voltage when *Q* is "off" but is approximately constant at 0.5 V when *Q* is "on." Both of these results make sense.

Measurement of the collector voltage from Q7 in the NorCal 40A is shown below. The measured collector voltage waveform is closer to a half-sinusoid than in the simulation shown above. The specific transistor has a big effect on the collector voltage, as it will in simulation.



Notice that the output voltage Vout is nearly a perfect sinusoid with a frequency equal to the source! The Harmonic Filter circuit has filtered out all of the "higher-ordered harmonics" and has left this nice sinusoidal voltage at the antenna input. Very, very cool!

Now, let's try to understand why the collector voltage has such a complicated shape. It's actually due to inductive kick and ringing, like you observed in Probs. 5 and 6! If the period were longer, the collector voltage might appear as



Maximum Efficiency of the Class C Power Amplifier

The text shows a simplified "phenomenological" model of this amplifier in Fig. 10.3(a). The collector voltage $V_c(t)$ (= V_s in Fig. 10.3) and current are:

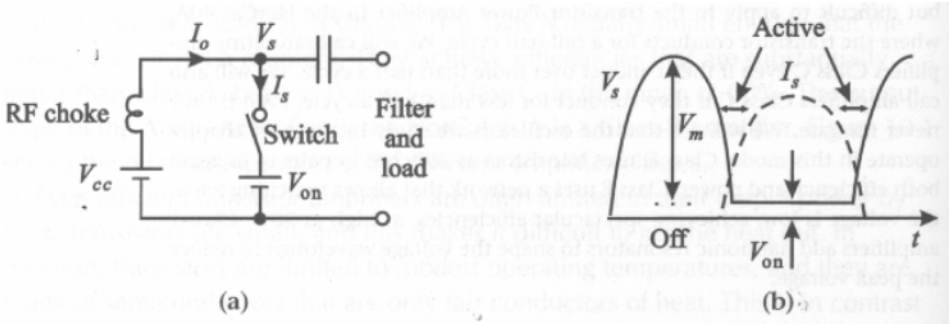


Figure 10.3. Switch model for the Class-C amplifier (a), and switch voltage V_s and current I_s waveforms (b).

According to this model

$$V_c(t) = V_s(t) = \begin{cases} V_{\text{on}} + V_m \cos(\omega t) & \text{switch open} \\ V_{\text{on}} & \text{switch closed} \end{cases} \qquad (10.1)$$

A key point is that the time average value of the collector voltage $V_c(t)$ must equal V_{cc} since RFC has zero resistance:

$$\frac{1}{T}\int_{t_0}^{t_0+T} V_c(t)\,dt = V_{\text{cc}}$$

We saw this effect earlier. If V_{on} is small with respect to V_m, then

$$V_{\text{cc}} = V_{\text{on}} + \underbrace{\frac{1}{T}\int_0^{T/2} V_m \cos(\omega t)\,dt}_{V_m/\pi} = V_{\text{on}} + \frac{V_m}{\pi} \qquad (10.2)$$

Therefore,

$$\boxed{V_m = \pi\left(V_{\text{cc}} - V_{\text{on}}\right) \ \text{[V]}} \qquad (10.3)$$

For example, with $V_{cc} = 12.8$ V and if $V_{on} = 2.6$ V, then $V_m = 32.0$ V. This compares well with the data shown earlier: $V_m = 31.6$ V from the ADS simulation and 33.2 V from my NorCal 40A measurements.

The dc power supplied by the source is

$$P_o = V_{cc} I_o \tag{10.4}$$

where I_o is the time average current from the supply.

Now, due to the blocking capacitor this same I_o flows through Q. If we assume Q is never active, then $V_c = V_{ce,sat} = V_{on}$ such that

$$P_d = V_{on} I_o \tag{10.5}$$

where P_d is the power dissipated in Q. (We're neglecting the power dissipated in the brief instant when Q is active as it transitions from saturation to cutoff, and vice versa.)

The remaining power must be dissipated in the load R as signal power, P:

$$P = \underbrace{P_o}_{(10.4)} - \underbrace{P_d}_{(10.5)} = V_{cc} I_o - V_{on} I_o = (V_{cc} - V_{on}) I_o \tag{10.6}$$

Consequently, the *maximum* efficiency η_{max} of this Class C amplifier is approximately

$$\eta_{max} = \frac{P}{P_o} \approx \frac{(V_{cc} - V_{on}) I_o}{V_{cc} I_o} = 1 - \frac{V_{on}}{V_{cc}} \tag{10.7}$$

Using $V_{on} = 2.6$ V from the previous page,

$$\eta_{\max} = 1 - \frac{2.6}{12.8} = 0.797 = 79.7\%$$

This value of $\eta_{\max}$ should be pretty close to your measured $\eta_{\max}$.

Lastly, where did this mysterious $V_{on} = 2.6$ V come from? I obtained this value from (10.3) using ADS and experiment. It was not analytically derived. This value is reasonable given the collector voltage measurement shown earlier.