Nonlinear Analysis, Simulation and Measurement of RF Amplifiers

Modeling an amplifier's linear response (gain and input match) is common, as is measurement of the finished circuit using vector network analyzers. However, it is now practical to simulate compression, distortion and other nonlinear effects in the design phase, and find them in close agreement with the measurements made when the amplifier is later built.

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Modeling the linear response of RF and microwave amplifiers such as gain or input match has been common practice from many years. Similarly, vector network analyzers (VNAs) are used to measure the S-parameters, allowing gain or input match to be displayed on a Smith chart. However, with further integration of systems, emphasis on lower cost, and lower-powered RF circuits, it is increasingly important to understand, predict, and measure compression, distortion and other nonlinear effects in these circuits.

New computer aided engineering programs employ SPICE models to predict nonlinear as well as linear performance.

New computer aided engineering systems employ the traditional SPICE models of RF components and apply a nonlinear analysis in the frequency domain to generate simulations such as power compression, harmonic distortion and intermodulation distortion. Enhanced presentation routines

can display not only the frequency response of the distortion, but also voltage waveforms as a function of time. They even trace out I-V operating points of a device in response to an RF signal. These tools not only facilitate circuit simulation, they provide insight into how the inside of a circuit operates in the large- signal, nonlinear domain. Most importantly, they provide this insight into the circuit at the engineering phase, before the network is actually built.

RF VNAs can be configured to measure several of the key nonlinear parameters. Power compression and harmonic distortion can be measured directly over a swept power range, or at a constant output power over a frequency range. Real time sweeps allow adjustment of bias to view the effect on these measurements and the results can be stored to a disk or read directly into a CAE system for comparison with predicted results.

This paper illustrates the basics of nonlinear simulation and measurement using as an example the Avantek MSA 0986 monolithic IC amplifier, analyzed and measured for gain, output power, 1-dB compression point and harmonic distortion. The approach is general to other manufacturers' products in that the data sheet models can be used to generate the linear and nonlinear subcircuits used in the simulations.

Network analysis of surface-mount technology (SMT) components reveals numerous parasitics. Complete characterizations have been performed to generate an SMT library of parts. This is extended to surface-mount components such as inductors, capacitors, and resistors and not only allows a design of a complete amplifier circuit but actually makes practical the extension of the useful frequency range of operation of the IC amplifier, as will be seen from the following design example.

A library of components and their detailed equivalent circuits makes possible such precise modeling that their frequency use limits are extended.

Linear and nonlinear simulation may include varying device parameters and bias points. Sweeping variables such as bias point, transistor beta, and input power generate data sheet-like curves from the model of the device. This allows analysis of nonlinear performance over a range of device process and circuit variations. The simulation and analysis may be presented in several useful forms including harmonics and power compression versus input power, and output power and harmonics versus frequency.

The final portion of this paper illustrates nonlinear measurements using a VNA. Simple calibration processes are used that result in real-time measurements of harmonics and gain compression. The simulated nonlinear performance of the amplifier will be compared to the measured data, which allows the reader to determine the quality of the simulations.

This paper represents the state-of-the-art in RF design technique, focuses on understanding the devices and circuits, and is written from the viewpoint that the prototype circuits should work the first time with very close to the design performance expectations.

Generating the Circuit Models

Suppliers of RF surface-mount amplifiers provide models and measured data for their devices. Using the linear models, the performance of the devices may be extended beyond their nominal range of usage. Careful modeling of surface-mount components and printed circuit board (PCB) layout permits precise prediction of circuit characteristics such as gain and match. Further, with the nonlinear SPICE model for the device, power compression and harmonic distortion can be simulated, and the operating point and circuit can be changed to optimize power performance.

In this example, the 50 MHz low frequency limit of the packaged IC amplifier was extended all the way down to 300 KHz.

In this example a broadband PCB amplifier is designed. While normally limited at the low frequency to 50 MHz, this design approach extended the low end to 300 kHz by adding a second feedback loop. Careful modeling and component selection ensured that the high frequency response was uncompromised by this extension. The harmonics and power compression were modeled and measured with remarkable agreement.

RF circuit design bridges the gap between low frequency analog and digital circuits, and high frequency microwave circuits. Components are often PC board mounted like a lumped circuit, but dis-

tributed effects require the application of microwave techniques.

The key to the amplifier circuit is the packaged silicon IC. The data sheet for this amplifier shows linear characteristics such as gain and input match, DC characteristics such as voltage versus current, and some nonlinear characteristics such as output power compression. But others, such as harmonics at given input or output power are not shown. Finally, the frequency range indicated by the data sheet as readily available when the IC is used alone was much less extensive than we desired. The IC has an excess gain from DC to about 50 MHz. We wish to have flat gain starting as low as 300 kHz.

However, the published data for the IC does include extensive modeling information including packaging effects, linear models and SPICE models. Using the HP RF Design System, we were able to evaluate designs for the low frequency extension, as well as evaluate the design for harmonics versus output power.

If the simulation matches measured results for power compression and harmonic distortion, then we may have some confidence that the power performance measured from the device is predictable. Once the modeling is verified, changes to the model such as might occur due to processing variation can be investigated to determine if acceptable circuit performance will be maintained over the expected variation in components. In this design, it was desired that the amplifier deliver at least +7 dBm with better than -25 dBc harmonic distortion.

A circuit using the IC amplifier along with ideal resistors and inductors was simulated as a starting point for the design. An initial simulation of the amplifier IC with only a bias resistor was performed. Then, a simple feedback circuit consisting of a series inductor and resistor was added to control the low-frequency gain and the simulation repeated. The results (Figure 1) reveal that the feedback extends the response uniformly to 300kHz, as desired, when the feedback network consists of ideal elements having no package parasitics. However the surface-mount components do have parasitics, as will be seen, and these too must be accommodated in the design.

The response of the amplifier IC shows a large gain increase below 50 MHz. Reference to the published data indicates that is caused by the limited frequency response of an internal feedback capacitor. When a low frequency feedback path is added, with the inductor to remove the second path when the internal feedback takes over, the low frequency gain inherent in the IC chip is regained. Even to obtain these simple, ideal circuit responses, a complete model of the IC amplifier, including both the IC chip and its package parasitics is needed (Figure 2).

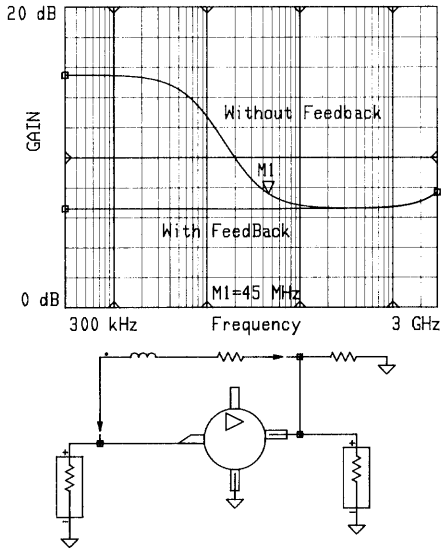

Figure 1. Response of the example IC amplifier in an ideal circuit with and without feedback to control low-end gain.

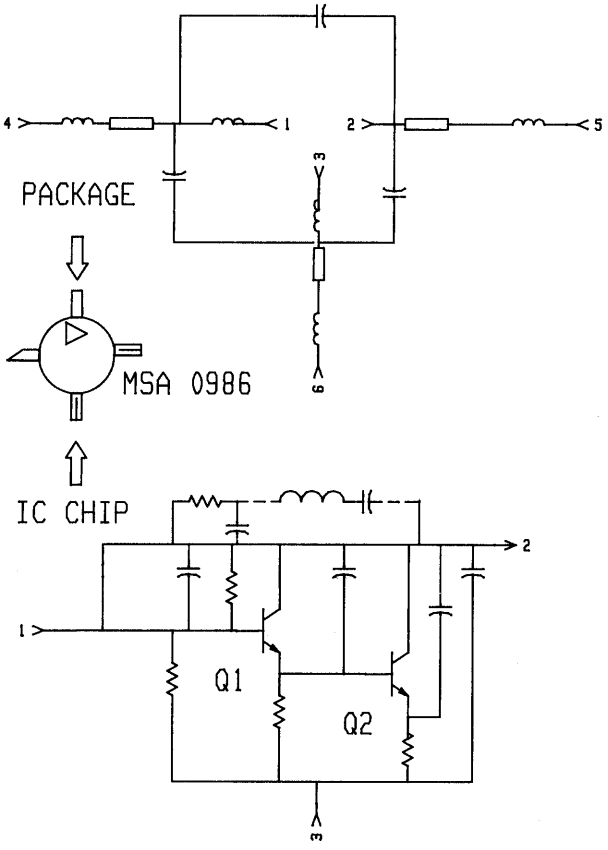

Figure 2. The amplifier model includes both the IC chip equivalent circuit as well as that of the parasitics of the package in which it is embedded.

We created a symbol for the packaged IC. It can be used as any other simulator part in a top-level circuit or as part of a more complex circuit. The IC amplifier subcircuit consists of two lower-level circuits. One is a general circuit for the plastic package. Any other transistor or IC device packaged in this same package could re-use this subcircuit. The second circuit is that of the IC chip, which might be procured in a variety of packages or in chip form. Separating the IC subcircuit separate from its package allows it to be re-used more conveniently in other applications.

IC Chip Model

The IC consists of various thin-film resistors and some parasitic capacitors, with two transistors. A given manufacturer might offer the same circuit with variations in the transistors that it contains, in which case one could make one subcircuit for the IC circuit and connect it to the transistor subcircuits. This model could be re-used for a family of IC types merely by changing the values for resistors and capacitors and adding the appropriate transistor model(s). Here we add the two transistors for the example amplifier, making the IC complete. These transistors, Q1 and Q2, use the same circuit model, with scaling factors and resistance values passed down into the model.

Modeling can be performed in blocks, as for the IC chip in one circuit and its package in another. This way the circuits can be reused, for example, when a different chip is placed in the modeled package.

In this amplifier, the linear model may be used for the transistors. There are two transistors of different sizes in the IC. We make only one model and pass in the scaling factor for the capacitances and resistance depending on the transistor. This model works well for linear simulations, but cannot be used for DC or harmonic generation simulations. However, for nonlinear analysis it is only necessary to replace the linear transistor model with a nonlinear model, developed next.

The nonlinear model for the transistor includes an ideal SPICE model transistor, surrounded by other elements such as diodes and resistors. The diodes are used to model the nonlinear capacitance effects of the device. The manufacturer's published data supplies all the necessary information to generate the model.

Complete Amplifier Design

A complete amplifier was designed using surface-mount part models and the IC part model. A secondary feedback path was added to control the low frequency gain. The inductor was chosen to remove the effect of the external low frequency feedback path at frequencies above which the internal feedback becomes significant. The simulation used the linear model to determine the small-signal response of the circuit. This design (Figure 3) is much more complete than the first ideal circuit, and includes blocking capacitors on the input, output and feedback paths, and resistors that were chosen to provide DC bias with sufficient power handling capacity. The parasitics of each of these parts may affect the circuit response substantially.

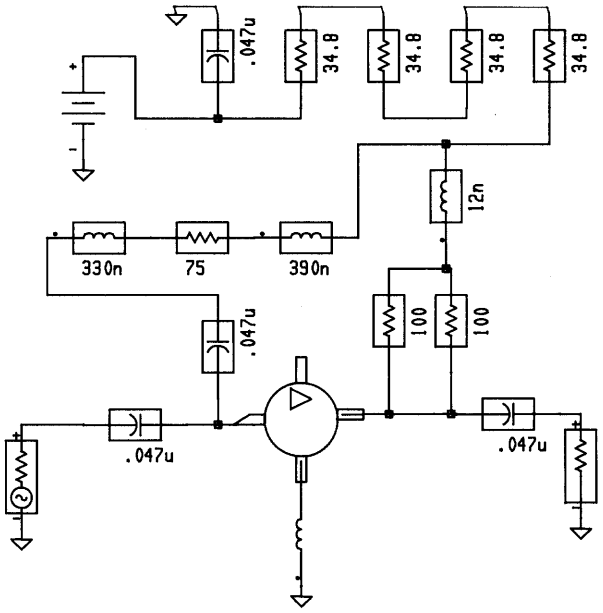

Figure 3. Complete amplifier with surface mount parts for feedback and bias.

Surface-Mount Models

The models of the surface-mount parts are key to the successful simulation of the circuit. Models for a wide range of surface-mount parts were developed using network analyzer data to match the characteristics to lumped circuit models. The parts are used by specifying the part value, which is linked to the particular values needed in the lumped model (Figure 4).

The Smith chart response of the actual inductor is shown in Figure 5, as measured on a VNA. Notice

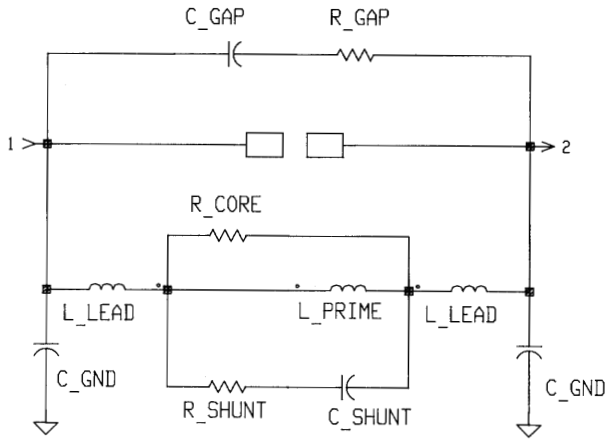

Figure 4. This complex circuit is used to model a library of surface-mount inductors of various values. Selecting the appropriate value (label) from the library evokes the respective parasitics for that part.

that at the low frequency, near 10 MHz, the inductive reactance is close to the value corresponding to the nominal inductance, as denoted by marker 0. The trace crosses the real (horizontal) axis at about 270 MHz. This is the primary resonance at which shunt capacitance and the inductance have a parallel resonance. Here the impedance of the part is very high and purely resistive. The component may, nevertheless, be useful as an RF choke.

Above this frequency, the part no longer performs as a simple inductor. On the Smith chart, resonances appear as circles or loops. The next resonance occurs at about 1 GHz, at which frequency the impedance of the part has decreased. Still another resonance appears as the frequency approaches 6 GHz.

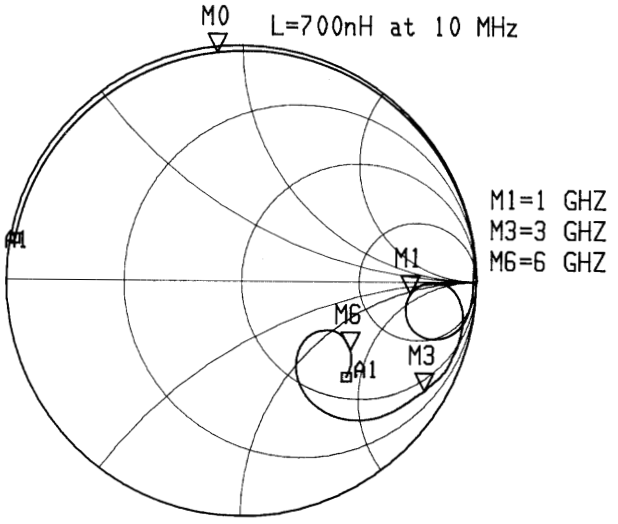

Figure 5. This Smith chart plot depicts the measurement of a 680 nH surface-mount inductor. Notice that it resonates near 270 MHz, 1 GHz and 6 GHz.

It is clear from the many resonances, which appear as circles or loops on the Smith chart, that a multi-element circuit model must be used to account for the high frequency response of this surface-mount inductor. Inductors usually require the most complex models, but surface-mount capacitors and resistors also exhibit high frequency behaviors requiring multi-element equivalent circuits for accurate high frequency characterization. A library of commonly used surface-mount parts contained within this design software is used by the designer to create the complete circuit.

Amplifier Simulation Response

The complete amplifier was simulated using the linear model, from which it was determined that, unlike the performance with an ideal external feedback inductor, when a surface mount inductor is used having its parasitic reactances, the low frequency gain is extended but the high frequency response is dramatically affected. This may be appreciated from the resonances observed with the practical, surface-mount inductor, for which a gain dip could be expected around 1 GHz.

The feedback circuit modeled with an ideal inductor extended the low frequency range at no penalty in the high frequency response, but a real inductor with parasitics deteriorated high frequency performance.

Since smaller inductors have much higher self-resonant frequencies, the 680 nH inductor was realized as two smaller, series connected inductors. Sometimes adding inductors in series, or capacitors in parallel, causes additional resonances, however their deleterious circuit effects may be mitigated by dissipation within or between them.

The simulator should show whether any resonances will occur. The parasitics of the surface-mount parts are not usually reproducible from part to part. Parasitics can vary by 50% or more. However, it is important to include more than the simple first-order model with only a shunt C (and a single resonance) since the parasitics responsible for higher frequency resonances may have a significant impact within the frequency domain of interest, and this sensitivity thereby will be discovered during the simulation.

When two smaller surface mount inductors of 330 nH and 390 nH replace the 680 nH inductor,

the low-frequency response is about the same, but the high frequency gain dip is removed. However, there is a significant roll-off of the high frequency response. For this reason a third, smaller inductor of 12 nH was added to the feedback circuit, having a self resonance above 1 GHz. The final circuit and results are shown in Figures 6 and 7.

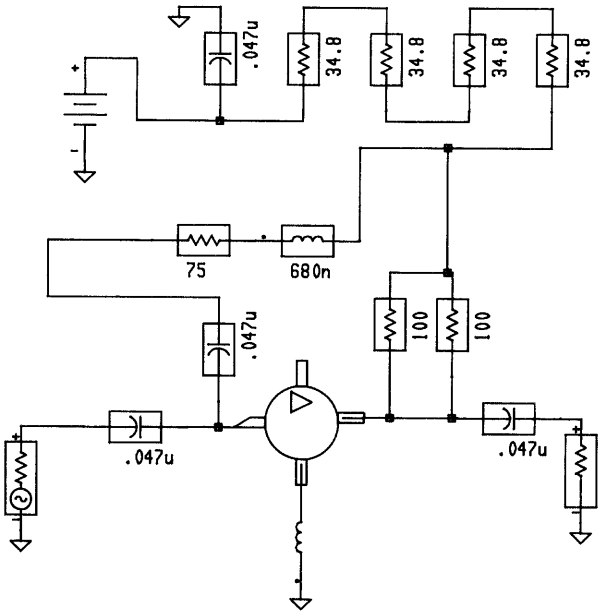

Figure 6. The circuit has a modified feedback network using two smaller inductors and an RF choke in the bias to improve high-end response.

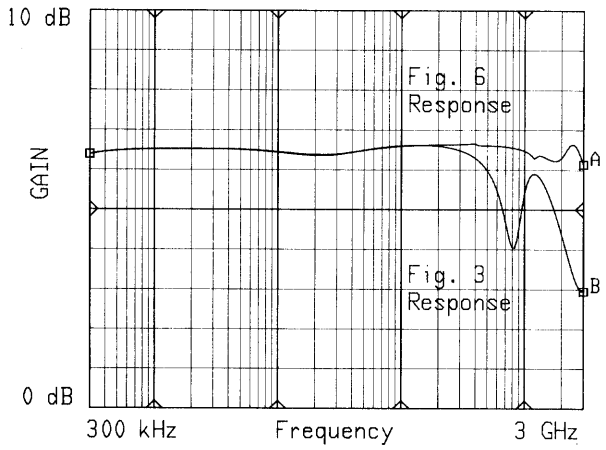

Figure 7. Amplifier response with the improvements of Figure 6.

Nonlinear Amplifier Simulation

Next, the nonlinear IC model was substituted for the linear model, in order to simulate DC and S-parameter behavior. Initial runs gave incorrect results for the bias point of the circuit. After estimating that a temperature rise was due to self-heating in the IC, the correct bias point was obtained, and the small- signal responses of the linear and nonlinear IC model agreed within about 0.3 dB over most of the frequency band.

The small signal response for the nonlinear circuit differs slightly at high frequencies from the linear response. Experience shows that the linear model often is better at predicting the small signal response, because it is optimized only for the small signal case. The nonlinear model may compromise the small signal response to predict more accurately the large signal performance. In this respect, which response is favored is at the designer's discretion. The DC voltages for the operating point agree very well with the actual measured values.

Simulation of the response of an amplifier to large signal power sweeps takes full advantage of the nonlinear simulator. The nonlinear analysis has been changed to a one-tone harmonic balance with a swept variable. The small signal input port has been replaced with a large signal power port (PLS). A stimulus block has been added to control the variable Pin, the input drive power. In this analysis, the fundamental and five harmonics are analyzed for each node in the circuit, at each power level.

The result of the analysis is shown in Figure 8. It is clear that the power compresses and will saturate below +15 dBm. This analysis was performed at 2 GHz, from which it is interesting to note the behavior of the second harmonic. Normally, a distortion signal will rise with input power as a function of its order, that is, a second harmonic will increase at two times the increase in input power, and a third harmonic will increase at three times. Here, the second harmonic follows that trend until the amplifier nears compression, beyond which the second

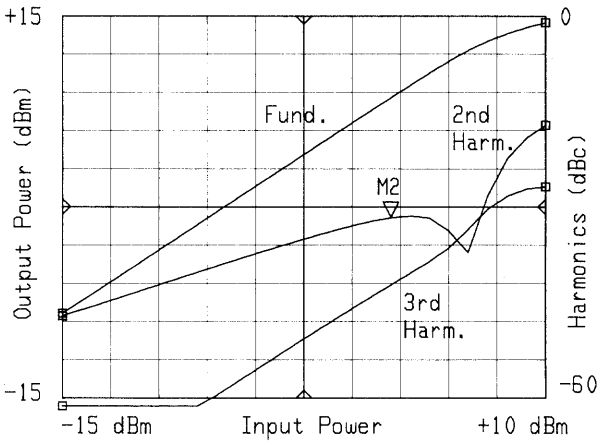

Figure 8. Simulated output power (in dBm) and harmonics (in dBc) versus input power (in dBm) at 2 GHz.

harmonic has a dip in its response. This may be due to the feedback in the amplifier, with the second harmonic cancelling itself at this frequency. It may also be that at these power levels the compression of the signal is symmetric, which suppresses even-order harmonic distortion. This affords a good opportunity to compare simulated results with actual measurement.

Measuring Nonlinear Responses

Using an RF network analyzer the power was swept while measuring gain and output power. In addition harmonics of the output were measured directly. The network analyzer was calibrated for power using a power meter in order to remove the effects of cables, fixtures and pads. In this way the accuracy of a VNA may be better than that of a power meter over a wide dynamic range. When the amplifier is added, the power compression, output power, and harmonic distortion for second and third harmonics can be shown. Further, the network analyzer data may be passed directly to the design software for comparison with calculated values.

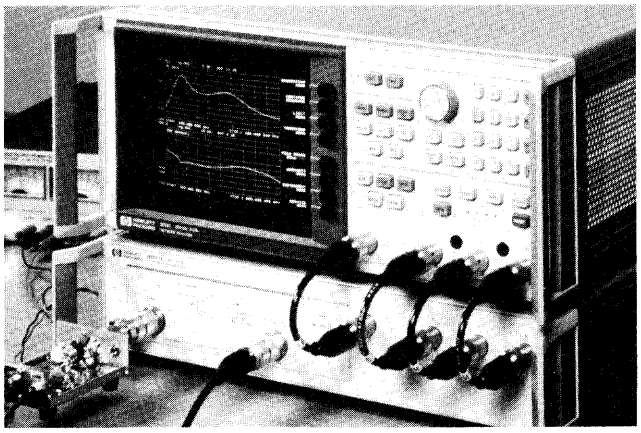

Figure 9. In addition to gain and match, the network analyzer can measure output power, power compression, and second and third harmonic distortion in real time.

The results measured for the breadboard circuit using the surface-mount capacitors and inductors in the feedback path are shown in Figure 10. The results agree well with the simulation. Remarkably, it predicts the dip in the second harmonic for a 2 GHz power sweep. The output power and compression point are within 1 dB of simulated. During the measurement bias may be adjusted while sweeping harmonics in real time to determine bias effects. In fact, this method is used to tune and minimize harmonic distortion of GaAs FET amplifiers used in the production of network analyzers made by our firm.

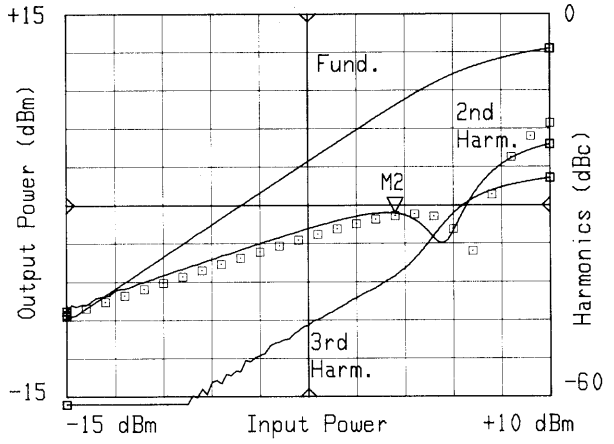

Figure 10. Measured power and harmonics for an IC amplifier (shown as solid line) and simulated second harmonics shown as boxes, at 2 GHz.

By performing power sweeps at different frequencies, we see that harmonic behavior and compression vary with frequency. By replacing the input power swept stimulus with a frequency swept stimulus and performing the harmonic balance analysis at each frequency, a swept harmonic simulation can be performed.

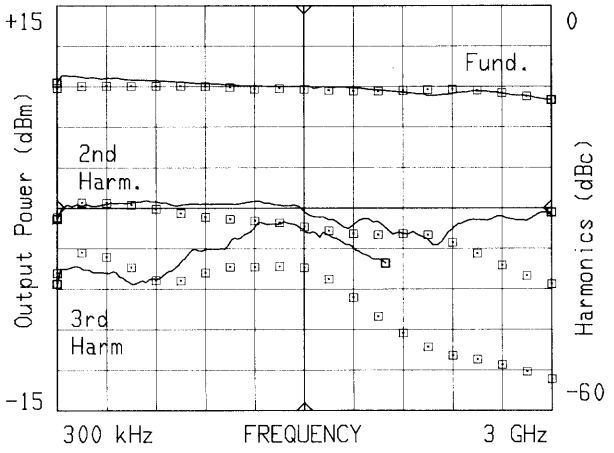

Figure 11. Measured (shown as solid line) and simulated (shown as boxes) power and harmonics versus frequency.

The harmonics versus frequency are shown in Figure 11. Also shown is the output power, all with a 3 dBm input signal. The second and third harmonics do vary several dB over frequency, with third harmonics getting worse at higher frequencies, up to about 1.5 GHz input. Above this frequency, the third harmonic is probably out of the gain region of the amplifier. We can now compare

this the response of a real amplifier, also shown in Figure 11.

The output power tracks the simulation remarkably well. Although the second harmonic does not show quite the roll-off of the model, the third harmonic shows a very similar response to the simulation. The third harmonic response is limited in frequency to 6 GHz (2 GHz fundamental) due to the frequency limit of the network analyzer used.

For measuring power parameters such as output power or 1 dB compression point, a VNA calibrated with a power meter is extremely accurate. Typical power accuracy better than 0.25 dB is easily achieved over a 50 dB power range. Very accurate gain measurement, even more so than power measurement, is necessary when determining compression points in amplifier measurements. Gain accuracy as good as 0.03 dB can be obtained with a suitably calibrated VNA.

From a practical measurement standpoint, the limitations in measuring harmonic distortion come from the harmonic content of the source and the distortion of the VNA receiver. Source harmonics in a limited band may be reduced by filtering the input signal. The receiver distortion is caused by a large fundamental signal, which generates harmonics in the receiver. Using a high- pass filter to remove the fundamental while passing the harmonics can improve the receiver harmonics without affecting receiver sensitivity. Padding the receiver input is a broadband way to reduce distortion, and is much like adding attenuation in a signal-analyzer measurement of harmonics. The maximum range of the receiver without filtering is about 60 dBc for harmonic measurements.

Observations

This application example demonstrates that the boundary of RF printed circuit boards can be stretched into the microwave region by using more complete circuit models for the parts and designing compensating networks for them as needed. It has been our experience from this and similar applications that surface mount parts can be used to 1.5 GHz and beyond if sufficient care in the modeling is taken. This includes modeling of all of the circuit elements, even ground inductance of vias and couplings in lines.

Equally important, using comprehensive, multi-element models of surface mount parts ensures proper consideration of their frequency limitations in the design process. Measuring results of both linear and nonlinear responses tie the design simulation and the real-world performance together. By careful consideration of the parts used, by creating models from manufacturers' data, by using measured data for individual parts when models are not available, and by using part libraries when available, RF circuit designs should yield measured linear and non-linear performance consistently close to that predicted on the first circuit realization attempt.

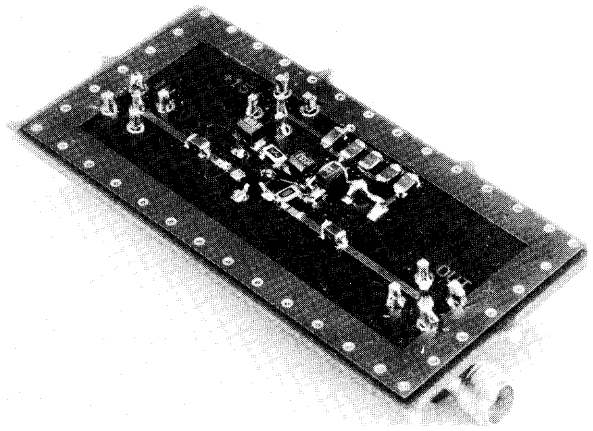

Figure 12. Photograph of a nearly complete surface mount amplifier circuit that is used for testing power-compression properties.

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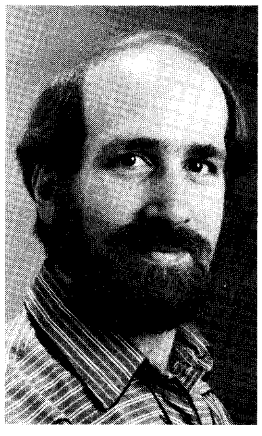

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